# 5-V Input, Variable Output, 20-A High-Efficiency Synchronous Buck Converter Using the UCC27222 with Predictive Gate Drive™ Technology

*Power Supply Control Products*

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## 1 Introduction

The UCC27222EVM–001 evaluation module (EVM) is a high-efficiency, synchronous buck converter providing a variable output between 0.9 V and 1.8 V at 20 A from a 5-V input. The EVM is able to start up from 5 V, so no additional bias voltage is required for start-up. The module uses the UCC27222 High-Efficiency Predictive Synchronous Buck Driver, along with the UCC3803 Low-Power BiCMOS Current-Mode PWM controller for demonstrating the Predictive Gate Drive™ (PGD) technique. Several advanced TI design and packaging technologies are used, providing the highest possible efficiency from step-down converters. Configured for voltage-mode control, the UCC27222EVM–001 operates at 500 kHz with a peak efficiency of 92%. Full load efficiency is just over 85% for $V_{OUT}$ = 1.8 V.

## 2 Description

The UCC27222 is the industry's first and only synchronous buck driver to include Predictive Gate Drive™ control technology. Predictive Gate Drive™ technology is a TI patented control technique that virtually eliminates body-diode conduction while also minimizing reverse recovery losses in synchronous rectifiers. This can result in significant synchronous rectifier switching efficiency improvements over competing technologies such as adaptive delay control or fixed delay.

Secondly, the UCC27222 3-A driver stage uses TI's unique TrueDrive™ hybrid Bipolar/CMOS output technology. The TrueDrive™ hybrid architecture consists of a mixed Bipolar MOS parallel output stage. To the user, this simply means ultra-fast rise and fall times by providing the highest possible drive current where it is needed most, at the MOSFET Miller plateau region.

The UCC27222 is available in TI's 14-pin PowerPAD™ package. PowerPAD™ is a thermally enhanced standard device package offering a three to five times improvement in power dissipation over similar standard device packages. With a junction-to-case thermal impedance of only 2°C/W, the UCC27222 requires no additional heatsink and can operate at much lower junction temperature resulting in increased component reliability.

The UCC27222EVM–001 highlights the many benefits of using the UCC27222 High-Efficiency Predictive Synchronous Buck Driver in conjunction with the UCC3803 Low-Power BiCMOS Current-Mode PWM controller. The following user guide provides the schematic, component list, assembly drawing, artwork and test set up necessary to evaluate the UCC27222 and UCC3803 in a typical synchronous buck application.

## 2.1 Applications

- Non-isolated 5-V input systems requiring high-efficiency and high-power density for very low output voltage, high-current converter applications, including:
- Processor power
- General computer
- Datacom
- Telecom
- Point-of-load DC/DC conversion from intermediate bus voltage

## 2.2 Features

- Up to 92% peak efficiency using the UCC27222 with Predictive Gate Drive™ technology
- 5-V typical input (4.5 V < $V_{IN}$ < 5.5 V)
- 0.9 V to 1.8 V variable output allows PGD evaluation at most popular VID voltages
- 20 $A_{DC}$ output current for 0.9 V < $V_{OUT}$ < 1.8 V
- High-frequency 500-kHz operation
- UCC3803 PWM control with low voltage 4.1 V start-up
- Single SO–8 MOSFET for upper and lower synchronous rectifier
- Compact size, low profile, surface mount design (2.4" x 2.1" x 0.4")
- Voltage-mode control
- Up to 100-kHz loop gain bandwidth for very fast transient response
- Double sided PCB with power stage and device's all on top side
- Convenient scope jacks for probing Predictive Gate Drive™ critical waveforms

# 3 Electrical Performance Specifications

**Table 1. Electrical Performance Specifications**

| PARAMETER | CONDITIONS | $V_{OUT}$ (V) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Input voltage range | | All | 4.75 | 5.00 | 5.50 | V |
| Maximum input current | $V_{IN}$ = 5 V, $I_{OUT}$ = 20 A | 0.9 | | 4.7 | | A |
| | | 1.2 | | 5.9 | | |
| | | 1.5 | | 7.2 | | |
| | | 1.8 | | 8.4 | | |
| No load input current | $V_{IN}$ = 5 V, $I_{OUT}$ = 0 A | 0.9 | | 90 | | mA |
| | | 1.2 | | 95 | | |
| | | 1.5 | | 98 | | |
| | | 1.8 | | 100 | | |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output voltage set | $V_{IN}$ = 5 V, 0 A ≤ $I_{OUT}$ ≤ 20 A | 0.9 | 0.89 | 0.90 | 0.91 | V |
| | | 1.2 | 1.19 | 1.20 | 1.22 | |
| | | 1.5 | 1.48 | 1.50 | 1.52 | |
| | | 1.8 | 1.78 | 1.80 | 1.82 | |
| Output voltage regulation | Line regulation (4.75 V < $V_{IN}$ < 5.5 A, $I_{OUT}$ = 0 A) | All | | | 1% | V |
| | Load regulation (0 A ≤ $I_{OUT}$ ≤ 20 A, $V_{IN}$ = 5 V) | All | | | 1% | |
| Output voltage ripple | $V_{IN}$ = 5 V, $I_{OUT}$ = 20 A | 0.9 | | 20 | | $mV_{P-P}$ |
| | | 1.2 | | 26 | | |
| | | 1.5 | | 31 | | |
| | | 1.8 | | 36 | | |
| Output load current | | All | 0 | | 20 | A |
| Output overcurrent | Limit source current to 10 A<br>Limit load current to 20 A | | | 0 | | |
| Output current limit | Limit source current to 10 A<br>Limit load current to 20 A | | | 0 | | |
| **CONTROL LOOP CHARACTERISTICS** | | | | | | |
| Switching frequency | | All | 450 | 500 | 550 | kHz |
| Control loop bandwidth | | | 60 | | 100 | |
| Phase margin | | | 30 | | 60 | ° |
| **EFFICIENCY** | | | | | | |
| Peak efficiency | $V_{IN}$ = 5 V, 6 A ≤ $I_{OUT}$ ≤ 10 A | 0.9 | | 85.5% | | |
| | | 1.2 | | 88.5% | | |
| | | 1.5 | | 90.5% | | |
| | | 1.8 | | 91.5% | | |
| Full load efficiency | $V_{IN}$ = 5 V, $I_{OUT}$ = 20 A | 0.9 | | 78% | | |
| | | 1.2 | | 82% | | |
| | | 1.5 | | 84% | | |
| | | 1.8 | | 85% | | |

# 4 Schematic

A schematic of the UCC27222EVM–001 is shown in Figure 1. Terminal block J5 is the 5-V input voltage source connector and terminal block J7 is the output and return for the 0.9 V to 1.8 V variable output voltage.

U1 is the UCC27222 shown with all the necessary discrete circuitry for high-efficiency operation. Q2 and Q3 are optimally selected based upon $R_{DS(on)}$, gate charge characteristics and input voltage requirements. In addition the synchronous rectifier, Q3 was chosen for dv/dt robustness. If the EVM is evaluated using Q2 and Q3 combinations different than originally configured, a small value (< 10 Ω) of R8 may be required to control inadvertent dv/dt induced turn-on of Q3.

Scope jacks J2 and J3 allow the user to measure the gate drive signals into Q3, the synchronous rectifier MOSFET and Q2, the upper control MOSFET. J4 allows convenient access to the drain-to-source voltage of Q3, also known as the switch node. J1 allows probing of the UCC3803 output. With R4 removed, the UCC3803 output can be measured while disabling the input to the UCC27222, and effectively running the controller without the power stage.

The UCC3803 is a current-mode PWM controller configured for voltage-mode control for this application. The controller is stabilized over all specified line and load conditions, with the internal error amplifier configured using a type 3 compensation scheme. Inserting a network analyzer between TP3 and TP4 allows convenient, non-invasive measurement of the control loop.

The EVM can be set to regulate to output voltages between 0.9 V and 1.8 V by varying the resistance of the trim pot, R11. R10 is a fixed 11-kΩ resistor in series with R11, so that when R11 is set to 0 Ω, the correct amount of voltage added, due to R10, to the FB pin of U2 forces the output to regulate at 0.9 V. Conversely, when R11 is set to the maximum value (50 kΩ), and added to R10, the resulting voltage added to the FB pin of U2, forces the output voltage to regulate at 1.8 V.

The output inductor, L1 is a 0.6-µH, 20-A inductor and is commonly available from various manufacturers. However, due to the differences in component design, and specific winding techniques there can be a significant variance in the DC winding resistance from one manufacturers part to another. When designing for high current output stages such as the UCC27222EVM–001, this can result in an efficiency gain or loss of as much as 1%. Therefore careful selection should be paid to properly select the optimal output inductor for a given synchronous buck application.

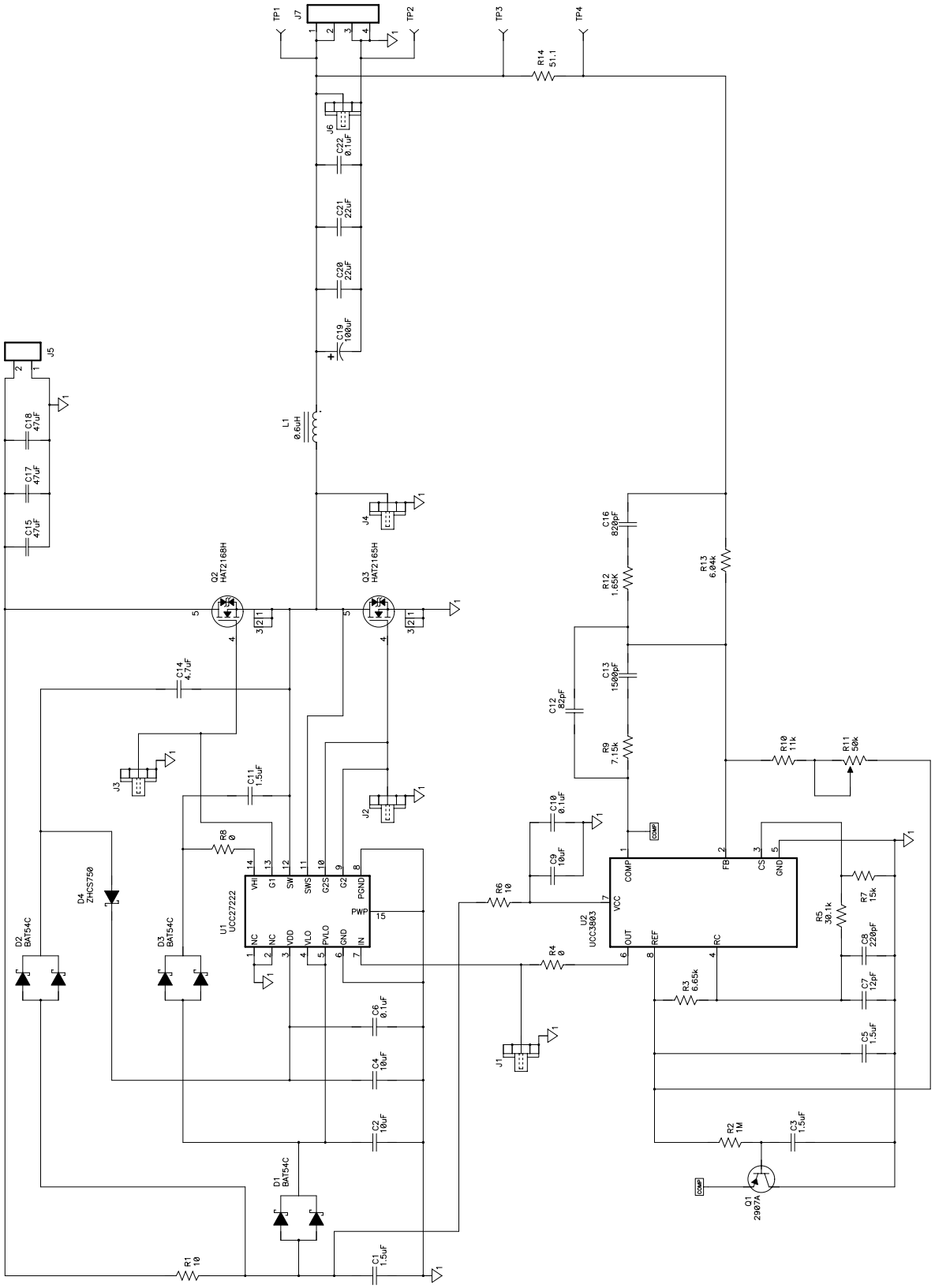



**Figure 1. UCC27222EVM–001 Schematic**

# 5 Variable Output Voltage

The output voltage of the UCC27222EVM–001 is variable between 0.9 V and 1.8 V, over the full range of the $V_{OUT}$-Adjust potentiometer, R11. By turning the $V_{OUT}$-Adjust knob all the way clockwise, the output voltage regulates at 1.8 V. Or, by rotating the $V_{OUT}$-Adjust knob completely counterclockwise, the output voltage regulates at 0.9 V. Intermediate voltages can be dialed in, by rotating the $V_{OUT}$-Adjust knob and monitoring the output voltage accordingly. Due to the 10 % tolerance of the potentiometer, it may not be possible, in some cases, to get exactly 1.800 V, or 0.900 V. Figure 2, shows graphically how $V_{OUT}$ varies as a function of the resistance of R11, making it simple to replace R11 with a fixed resistor for a given fixed output voltage. Resistors R10 and R11 combine to function as the output divider's pull-up resistance.

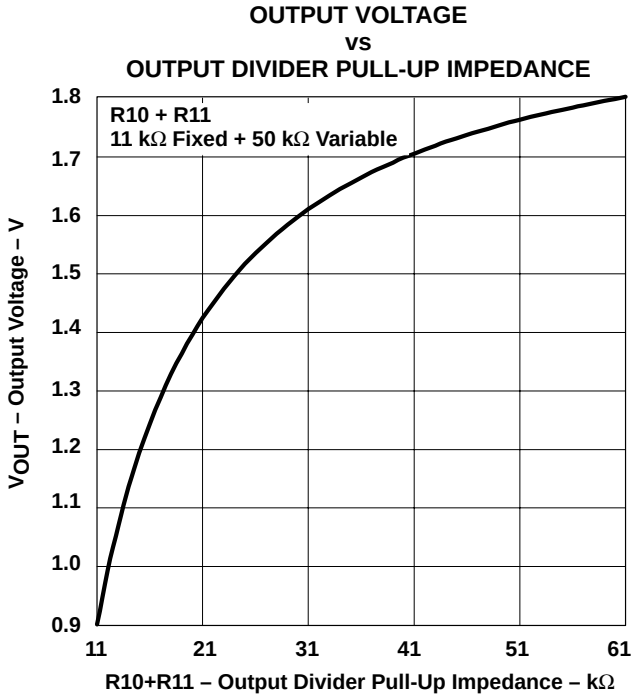



**Figure 2.**

**CAUTION:**

**Output voltage should be varied only while $V_{IN}$ is with the limits specified in Table 1, and $I_{OUT}$ is 0 $A_{DC}$. High currents flowing between the source voltage and the EVM, and between the output load and the EVM result in significant voltage drops through these connections. Varying the output voltage under heavy load can cause the input voltage to fall out of spec during maximum load current.**

# 6 Test Set Up

Shown in Figure 3 is the basic test set up recommended to evaluate the UCC27222EVM–001. Please note that although the return for J5 is the same as the J7 return, the VIN and LOAD1 connections should remain separate as shown below.

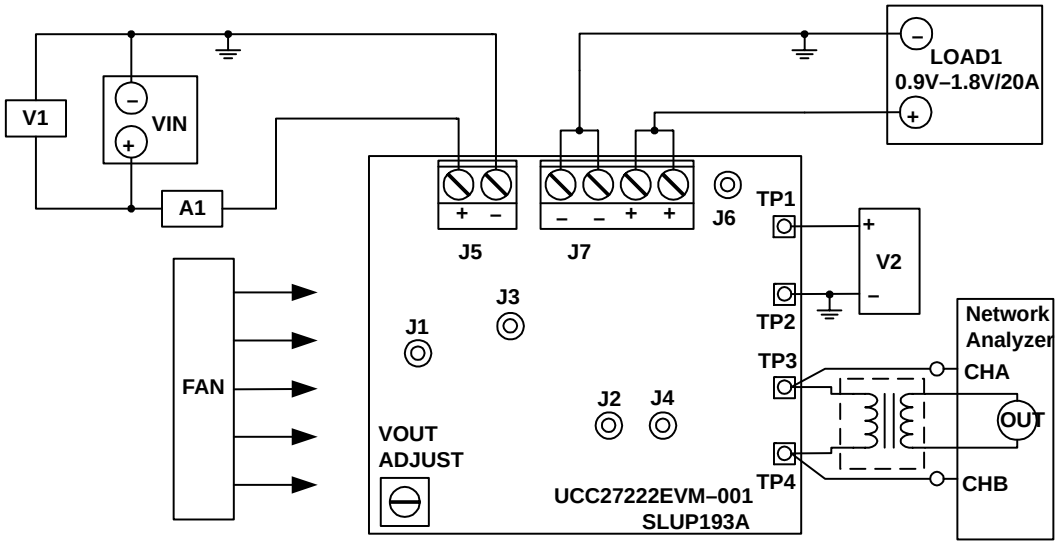



**Figure 3. Recommended EVM Test Configuration**

## 6.1 Ouptut Load (LOAD1)

For the output load to $V_{OUT}$, use a programmable electronic load set to constant current mode and capable of sinking 0 $A_{DC}$ to 20$A_{DC}$. Using a dc voltmeter, V2, it is also advised to make all output voltage measurements directly at TP1 and TP2 terminals. Measuring $V_{OUT}$ at LOAD1 or J7 results in some voltage measurement error, especially at higher load current, due to finite voltage drops across J7 and the wires between J7 and the electronic load.

**CAUTION:**

**The UCC27222–001 EVM does not provide output overcurrent protection. In order to avoid possible damage to the EVM, it is recommended to limit the maximum load current to 20 $A_{DC}$.**

## 6.2 DC Input Source (VIN)

The input voltage shall be a variable DC source capable of supplying between 0 Vdc and 6 Vdc at no less than 10 Adc, and connected to J5 as shown in figure 3. For fault protection to the EVM, good common practice is to limit the source current to no more then 9 $A_{DC}$ for a 5-V input. A dc ammeter, A1 should also be inserted between VIN and J5 as shown in Figure 2.

## 6.3 Network Analyzer

A network analyzer can be connected directly to TP3 and TP4 as shown in Figure 3. The UCC27222EVM–001 provides a 51.1-Ω resistor (R14) between the output and the voltage feedback to allow easy non-invasive measurement of the control to output loop response.

## 6.4 Recommended Wire Gauge

The connection between the source voltage, VIN and J5 of the EVM can carry as much as 10 $A_{DC}$. The minimum recommended wire size is AWG #18 with the total length of wire less than 8 feet (4 feet input, 4 feet return). The connection between J7 of the EVM and LOAD1 can carry as much as 20 $A_{DC}$. The minimum recommended wire size is AWG #16, with the total length of wire less than 8 feet (4 feet output, 4 feet return).

## 6.5 Oscilloscope Probe Test Jacks

J1, J2, J3, J4 and J6 are available to allow accurate probing and measuring of high speed noise sensitive signals such as gate drive voltage, switch-node voltage and output voltage ripple. The measurements that must be made to understand Predictive Gate Drive™ technology involve waveforms that are dithering within a 10-ns window. Using the pigtail ground lead commonly found on most oscilloscope probes results in unreliable measurements.

## 6.6 Fan

Most power converters include components that can get hot to the touch when approaching temperatures of 60°C. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200–400 LFM is recommended to reduce component temperatures when operating at or above 50% maximum rated load current.

# 7 Power Up/ Power Down Test Procedure

The following test procedure is recommended primarily for power up and shutting down the EVM. Whenever the EVM is running above an output load of 10 $A_{DC}$, the fan should be turned on. Also, never walk away from a powered EVM for extended periods of time.

1. Working at an ESD workstation, make sure that any wrist straps, boot straps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, $V_{IN}$, it is advisable to limit the source current from $V_{IN}$ to 9-A maximum. Connect the ammeter A1 (0-A to 10-A range) between $V_{IN}$ and J5 as shown in Figure 3. Make sure $V_{IN}$ is initially set to 0 V.
3. Connect LOAD1 to J7 as shown in Figure 3. Set LOAD1 to constant current mode to sink 0 $A_{DC}$ before $V_{IN}$ is applied.
4. Connect the voltmeter, V2 to TP1 and TP2 as shown in Figure 3.
5. Increase $V_{IN}$ from 0 V to 5 $V_{DC}$, while monitoring the output voltage on V2. $V_{OUT}$ should be in regulation when $V_{IN}$ > 4.1 V.
6. Vary LOAD1 anywhere between 0 A to 20 $A_{DC}$, making sure to turn on fan blowing air directly on the EVM for loads above 10 A.
7. Vary the input voltage between 4.5 V and 5.5 V.
8. Vary the $V_{OUT}$-Adjust over the full range to verify that the output voltage changes accordingly.
9. Shut down the electronic load.
10. Shut down $V_{IN}$.

# 8 Predictive Gate Drive™ Technology

## 8.1 Expected Efficiency Improvement with the UCC27222EVM–001

The benefits of Predictive Gate Drive™ technology become more significant at higher frequency and lower output voltage. For a synchronous buck converter, operating under similar specifications as shown in Table 1, but not employing Predictive Gate Drive™ technolgy, a total synchronous rectifier body-diode conduction time of as much as 120 ns can exist. Due to the reduction in body-diode conduction time, the UCC27222EVEM–001 demonstrates a significant savings in the amount of power dissipated in the synchronous rectifier, Q3.

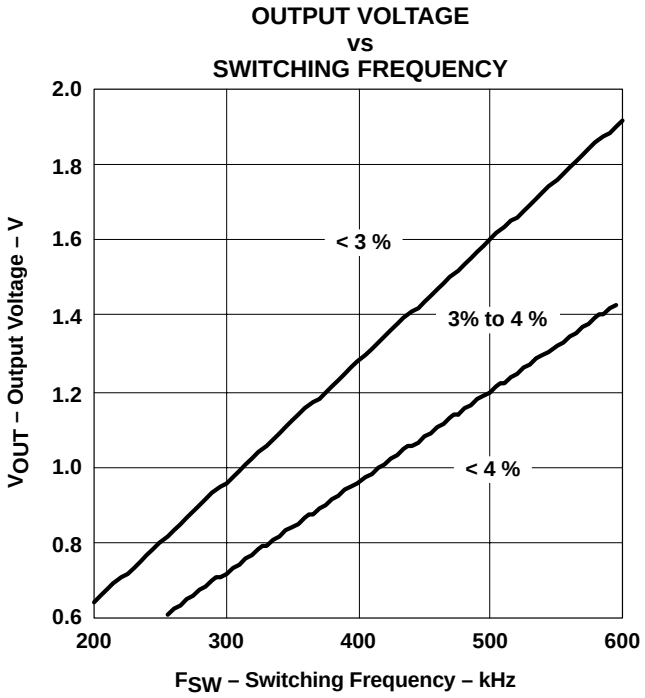



**Figure 4.**

In terms of overall efficiency gain, the graph shown in Figure 4 summarizes the amount of benefit that can be expected from the UCC27222EVM–001 with Predictive Gate Drive™ control, compared to a similar design not using Predictive Gate Drive™ control technology. The UCC27222EVM–001 operates at 500 kHz. Referring to Figure 4, at 500 kHz, when the output voltage of the UCC27222EVM–001 is adjusted to less than 1.2 V, a 4% increase in overall converter efficiency can be expected. Similarly, a 3% to 4% increase can be expected for 1.2 V < $V_{OUT}$<1.6 V, and an increase of slightly less than 3% is typical for 1.6 V < $V_{OUT}$ < 1.8 V.

## 8.2 Predictive Gate Drive™ In Action

All waveforms shown in Figures 5 through 8, were recorded with $V_{IN}$ = 5 V, $V_{OUT}$ = 1.8 V and $I_{OUT}$ = 20A. Using Tektronix P6138 or equivalent oscilloscope probes, inserted into J2 and J3 of Figure 2, the complementary gate drive signals of Q2 and Q3 shown in Figure 5 can be observed. Extremely fast rise and fall times as well as the minimal near zero delay between Q3 turn-off and Q2 turn-on should also be noted. Some dithering on the rising edge of Q2 and Q3 can be observed. A characteristic of Predictive Gate Drive™ technolgy, dithering should be nearly constant and limited to within a 10 ns window during the time that body-diode conduction would be occurring in Q3.

J4 of figure 3 allows convenient probing of the switch-node voltage, shown in Figure 6. The ringing shown on the switch-node voltage waveform is a result of component package inductance and parasitic inductance between the UCC27222 driver device and the high-speed switching MOSFETs, and is not a characteristic of Predictive Gate Drive™ technolgy. Predictive Gate Drive™ technolgy minimizes body-diode conduction as highlighted at points A and B of Figure 6. Figure 7 and Figure 8 show close up views of points A and B shown in Figure 6. Figure 8 shows some inductive ringing below the ground reference; however, it is not clamped by the body-diode of Q3.

# 9 Performance Data and Characteristic Curves

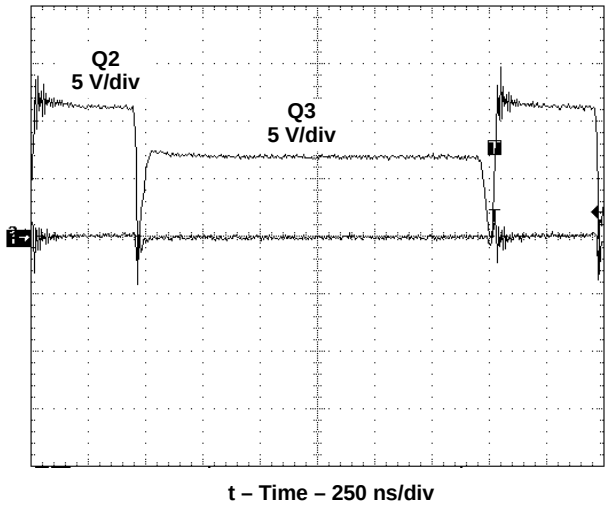



**Figure 5. Complementary Gate Drive Voltage**

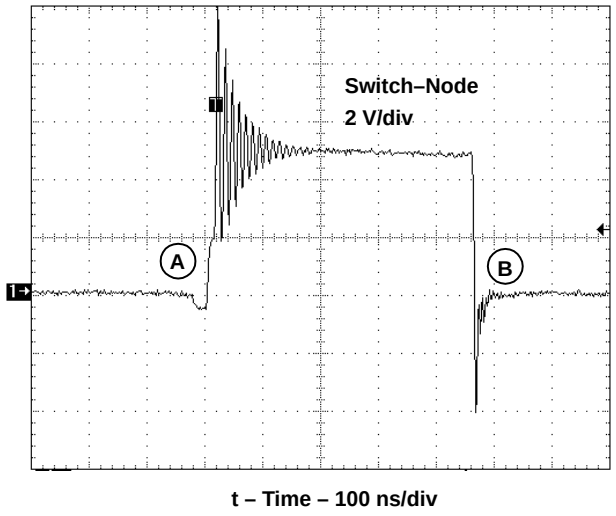



**Figure 6. Switch-Node Voltage**

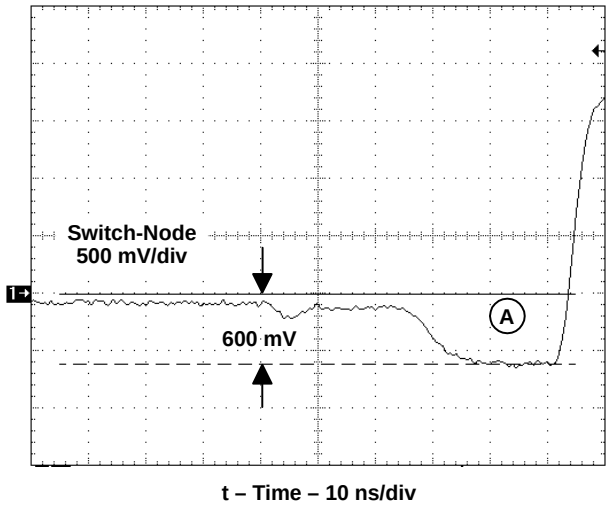



Figure 7. Close Up: Switch-Node A

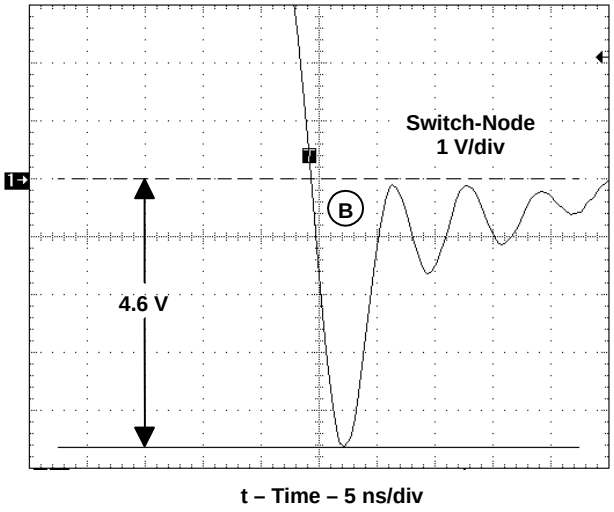



Figure 8. Close Up: Switch-Node B

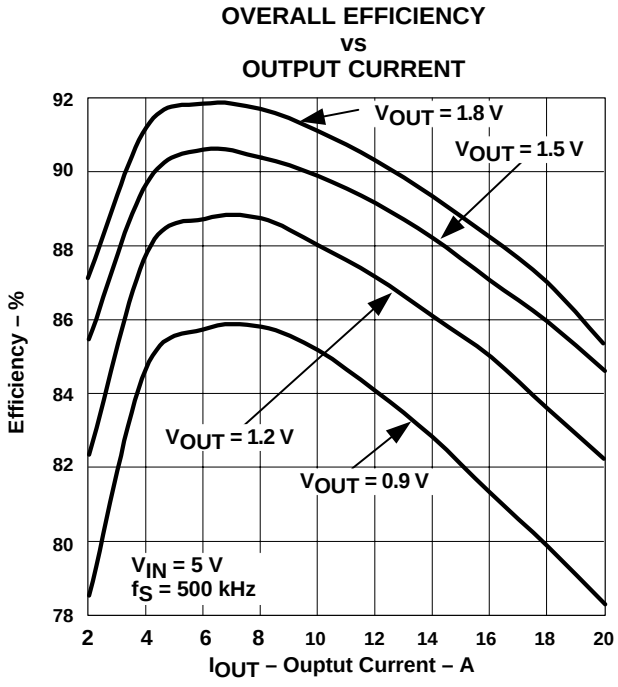



Figure 9.

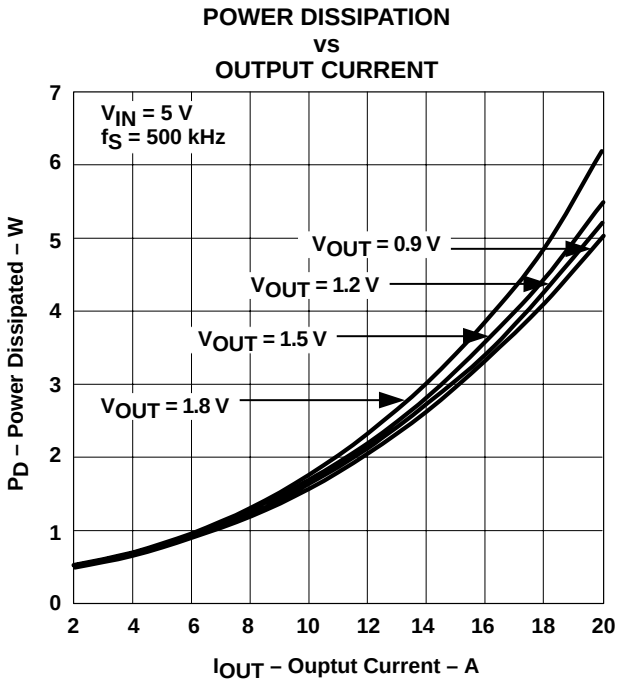



Figure 10.

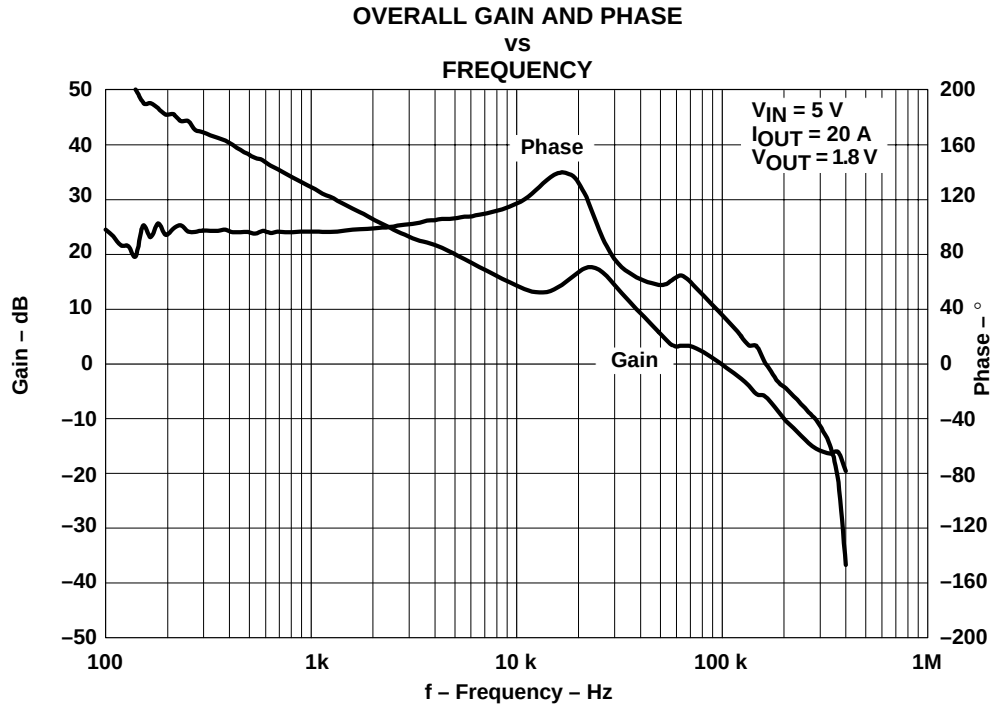



**Figure 11.**

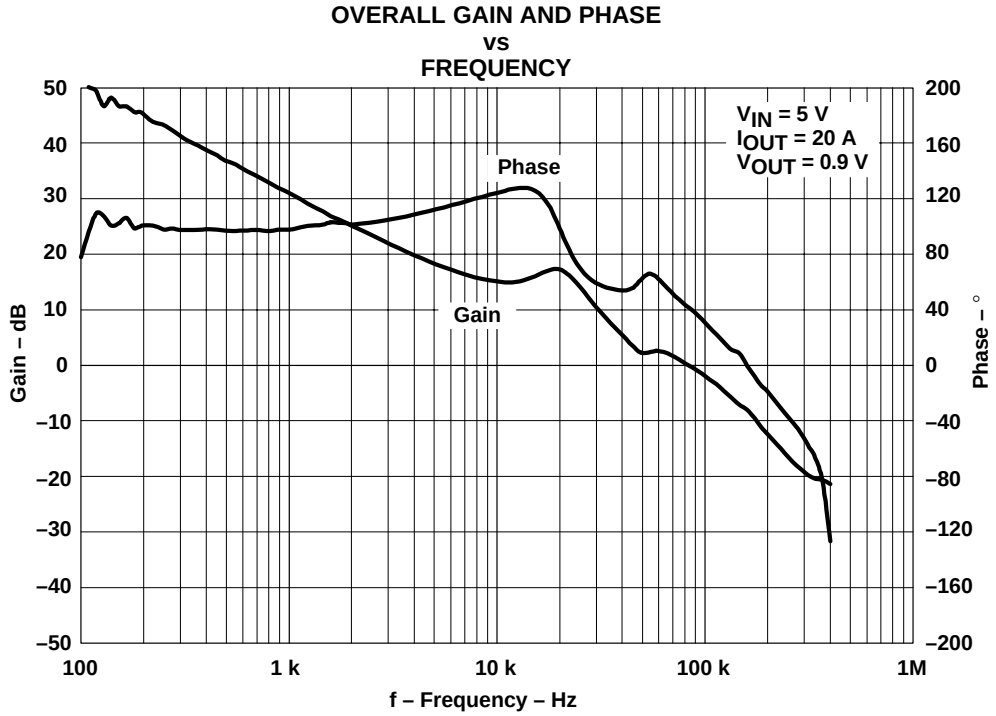



**Figure 12.**

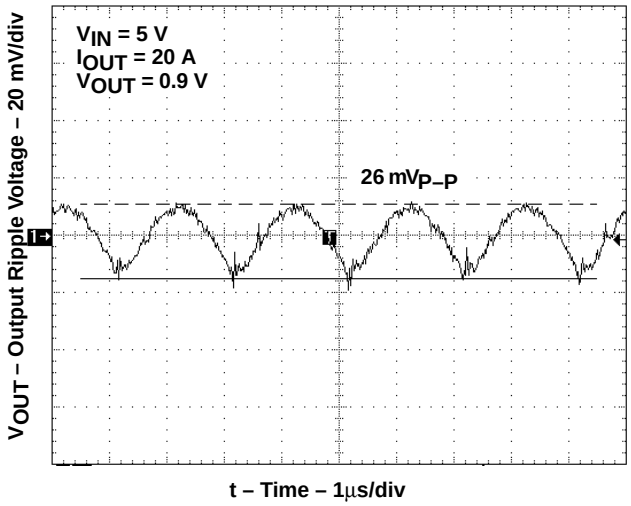



**Figure 13. Output Ripple Voltage**

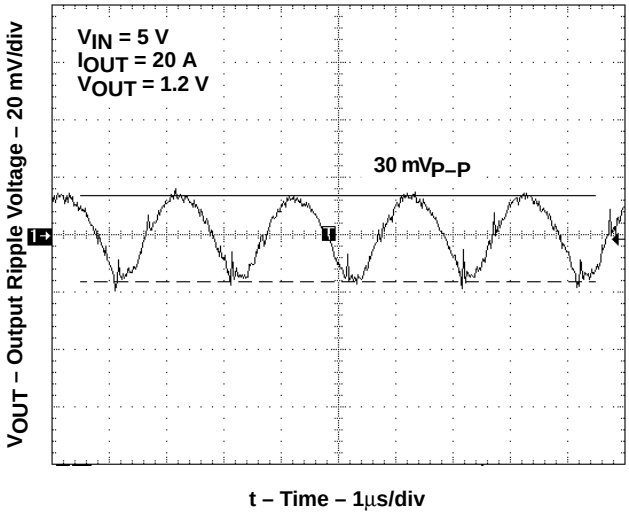



**Figure 14. Output Ripple Voltage**

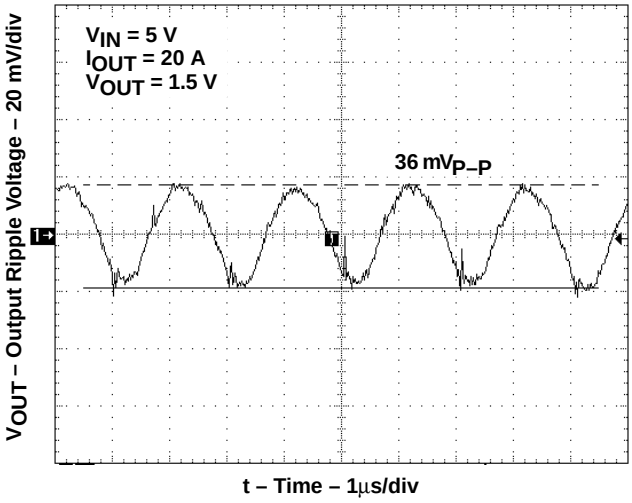



**Figure 15. Output Ripple Voltage**

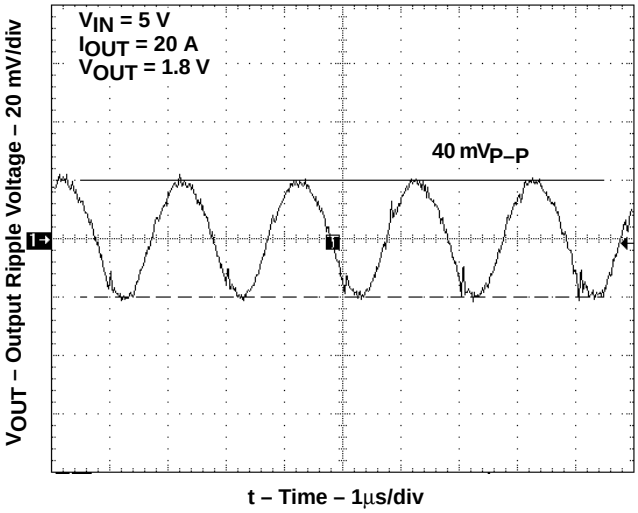



**Figure 16. Output Ripple Voltage**

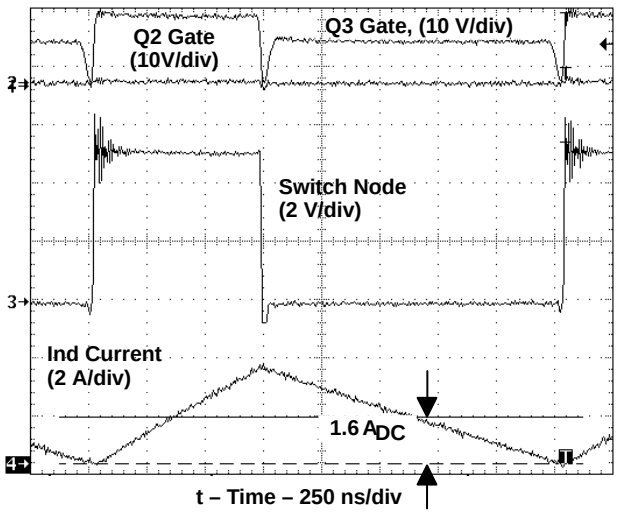



**Figure 17. PGD Start Threshold**

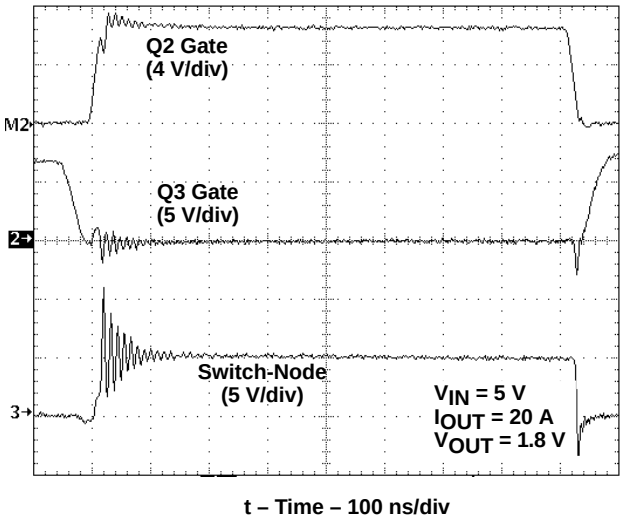
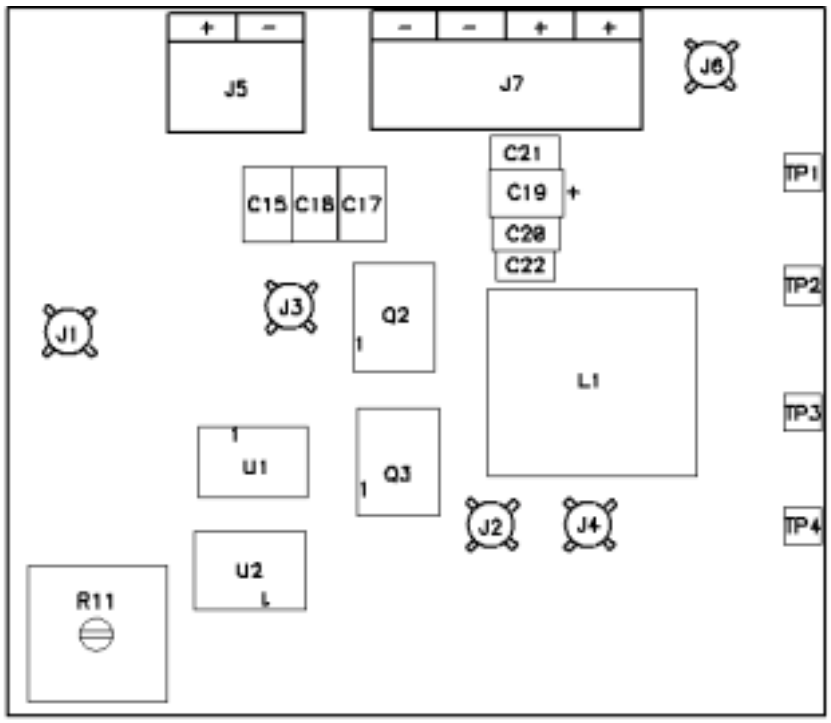
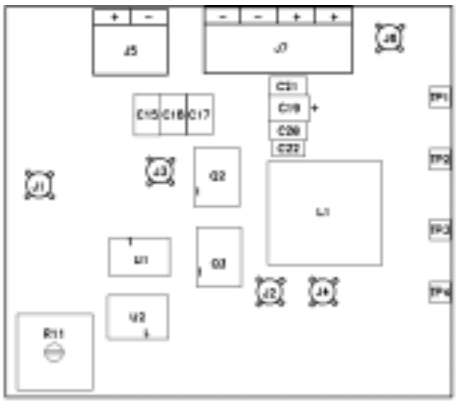



**Figure 18.**

## 10 EVM Assembly Drawing and Layout

Figures 19 and 24, show the top and bottom-side component placement for the EVM, as well as device pin numbers where necessary. A four layer PCB was designed using the top and bottom layers for signal traces and component placement along with an internal ground plane. The PCB dimensions are 2.1” x 2.4” with a design goal of maintaining all components to less than 0.5” high measured between the top and bottom layers. All components are standard OTS surface mount components placed on the both sides of the PCB. The copper-etch for each layer is also shown.



(Actual Size)

**Figure 19. Top Side Component Assembly**

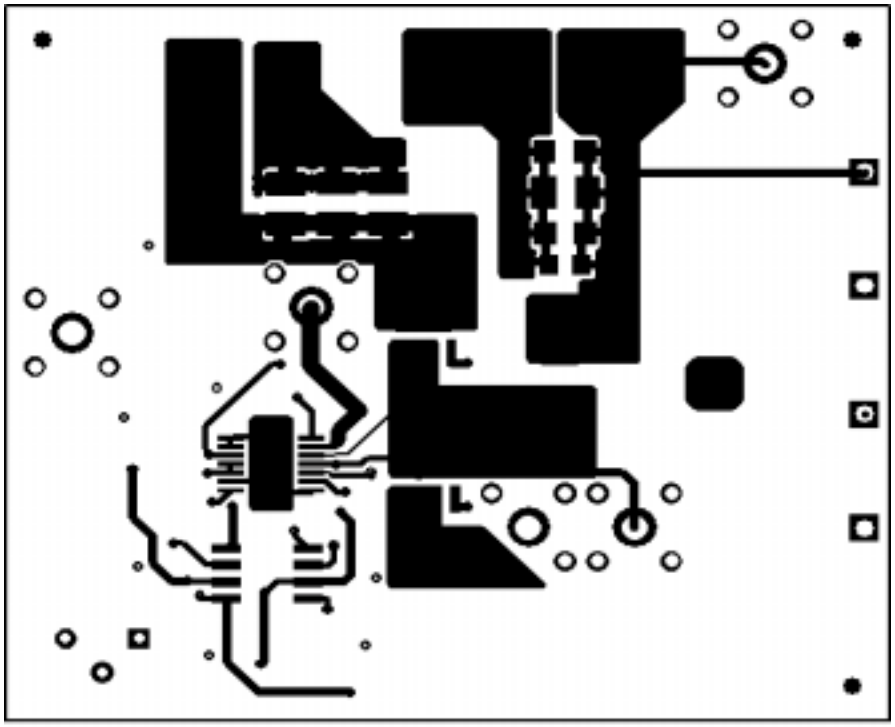


**Figure 20. Top Signal Trace Layer**

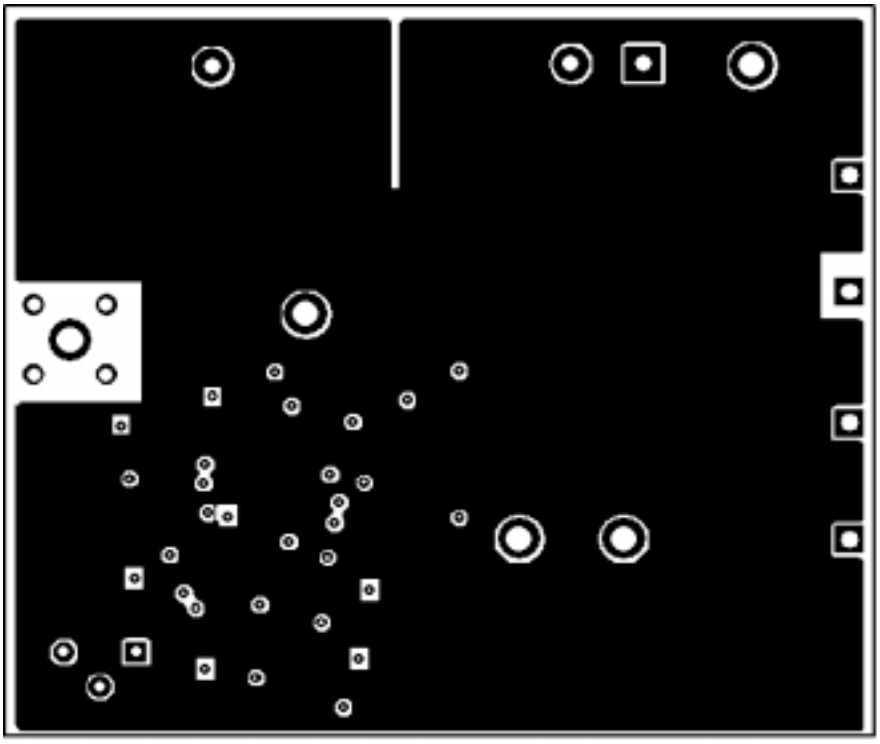


**Figure 21. Internal Ground Plane**

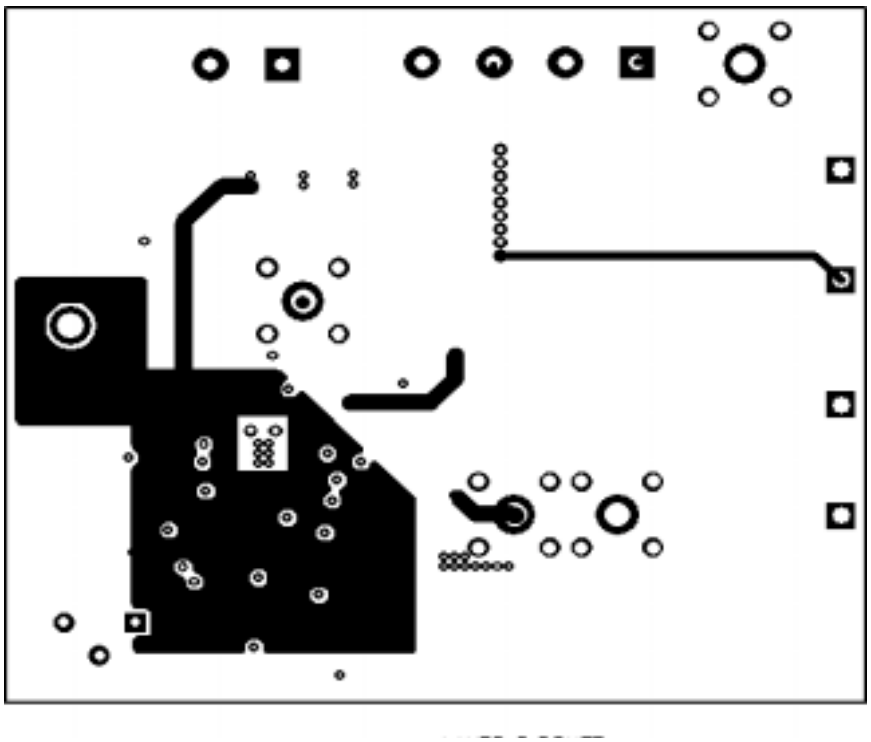


**Figure 22. Internal Signal Ground and Trace Layer**

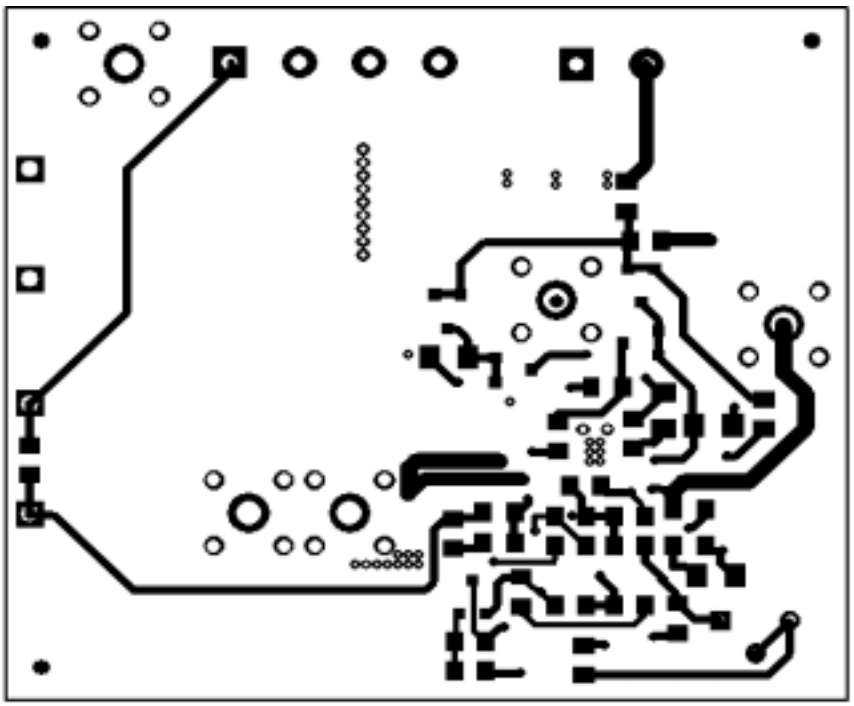


**Figure 23. Bottom Signal Trace Layer**

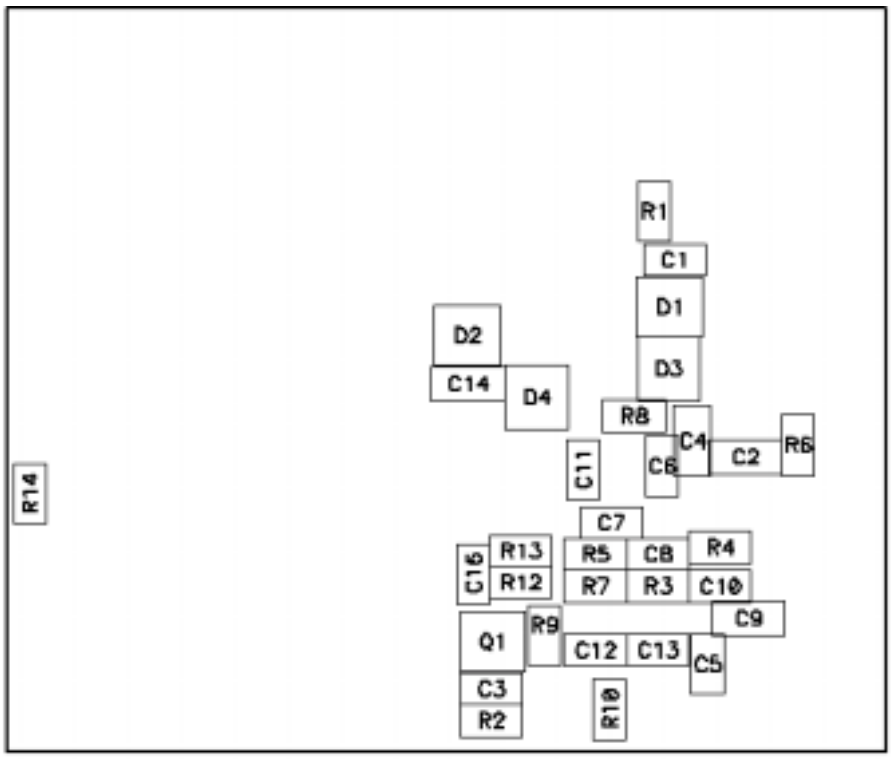



**Figure 24. Bottom Side Component Assembly**

# 11 List of Materials

Table 2 lists the EVM components as configured according to the schematic shown in Figure 1.

**Table 2. UCC27222EVM–001List of Materials**

| REFERENCE DESIGNATOR | QTY | DESCRIPTION | SIZE | MFR | PART NUMBER |
|---|---|---|---|---|---|
| C1, C3, C5, C11 | 4 | Capacitor, ceramic, 1.5 μF, 10 V, X5R, 20% | 805 | TDK | C2012X5R1A155M |
| C2, C4, C9 | 3 | Capacitor, ceramic, 10 μF, 10 V, X5R, 20% | 1206 | TDK | C3216X5R1A106M |
| C6, C10, C22 | 3 | Capacitor, ceramic, 0.1 μF, 25 V, X7R, 20% | 805 | Std | Std |
| C7 | 1 | Capacitor, ceramic, 12 pF, 50 V, NPO, 5% | 805 | Std | Std |
| C8 | 1 | Capacitor, ceramic, 220 pF, 50 V, NPO, 5% | 805 | Std | Std |
| C12 | 1 | Capacitor, ceramic, 82 pF, 50 V, NPO, 5% | 805 | Std | Std |
| C13 | 1 | Capacitor, ceramic, 1500–pF, 50 V, NPO, 5% | 805 | Std | Std |
| C14 | 1 | Capacitor, ceramic, 4.7 μF, 16 V, X7R, 10% | 1206 | TDK | C3216X7R1C475K |
| C15, C17, C18 | 3 | Capacitor, ceramic, 47 μF, 6.3 V, X5R, 20% | 1210 | TDK | C3225X5R0J476M |
| C16 | 1 | Capacitor, ceramic, 820 pF, 50 V, NPO, 5% | 805 | Std | Std |
| C19(1) | 1 | Capacitor, POSCAP, 100 μF, 4 V, 70 mΩ, 20% | B | Sanyo | 4TPB100M |
| C20, C21 | 2 | Capacitor, ceramic, 22 μF, 6.3 V, X5R, 20% | 1206 | TDK | C3216X5R0J226M |
| D1, D2, D3 | 3 | Diode, dual Schottky, 200 mA, 30 V | SOT–23 | Vishay | BAT54C |
| D4 | 1 | Diode, Schottky, 750 mA, 40 V | SOT–23 | Zetex | ZHCS750 |
| J1, J2, J3, J4, J6 | 5 | Adaptor, 3.5 mm probe clip (or 131–5031–00) | 3.5–mm | Tektronix | 131–4244–00 |
| J5 | 1 | Terminal block, 2 pin, 15 A, 5.1 mm | 0.40 x 0.35 | OST | ED500/2DS |
| J7 | 1 | Terminal block, 4 pin, 15 A, 5.1 mm | 0.80 x 0.35 | OST | ED500/4DS |
| L1(1) | 1 | Inductor, SMT, 0.6 μH, 22–A, 0.6 mΩ | PG0006 | Pulse | PG0006.601 |
| Q1 | 1 | Bipolar, PNP, 60 V, 600 mA | SOT–23 | Vishay | MMBT2907A |
| Q2(1) | 1 | MOSFET, N-channel, 30 V, 30 A, 6 mΩ | LFPAK | Renesas (Hitachi) | HAT2168H |
| Q3(1) | 1 | MOSFET, N-channel, 30–V, 55 A, 2.5 mΩ | LFPAK | Renesas (Hitachi) | HAT2165H |
| R1, R6 | 2 | Resistor, chip, 10 Ω, 1/10 W, 1% | 805 | Std | Std |
| R2 | 1 | Resistor, chip, 1M Ω, 1/10 W, 1% | 805 | Std | Std |
| R3 | 1 | Resistor, chip, 6.65 kΩ, 1/10 W, 1% | 805 | Std | Std |
| R4, R8 | 2 | Resistor, chip, 0 Ω | 805 | Std | Std |
| R5 | 1 | Resistor, chip, 30.1 kΩ, 1/10 W, 1% | 805 | Std | Std |
| R7 | 1 | Resistor, chip, 15 kΩ, 1/10 W, 1% | 805 | Std | Std |
| R9 | 1 | Resistor, chip, 7.15 kΩ, 1/10 W, 1% | 805 | Std | Std |
| R10 | 1 | Resistor, chip, 11 kΩ, 1/10 W, 1% | 805 | Std | Std |
| R11(1) | 1 | Resistor, trim potentiometer, 50 kΩ, 10% | 0.375 sq | Bourns | 3386P–1–503T |
| R12 | 1 | Resistor, chip, 1.65 kΩ, 1/10 W, 1% | 805 | Std | Std |
| R13 | 1 | Resistor, chip, 6.04 kΩ, 1/10 W, 1% | 805 | Std | Std |
| R14 | 1 | Resistor, chip, 51.1 Ω, 1/10 W, 1% | 805 | Std | Std |
| TP1, TP2, TP3, TP4 | 4 | PCB pin, 0.043 hole, 0.3 Length | | Mill–Max | 3103-1-00-15-00-00-0X-0 |
| U1(1) | 1 | IC, predictive synchronous buck driver | TSSOP–14 | TI | UCC27222PWP |
| U2(1) | 1 | IC, low-power BiCMOS current-mode PWM | SO8 | TI | UCC3803D |
| | 1 | PCB, FR4, 2.4” x 2.1” x 0.062” | 2.4 x 2.1 | Any | SLUP193 |
| | 4 | Bumpon, transparent, 0.44” x 0.2” | 0.44” x 0.2” | 3M | SJ5303 |

(1) Should not be substituted.

# 12 References


1. UCC27222 High-Efficiency Predictive Synchronous Buck Driver data sheet, (SLUS486)
2. UCC3803 Low-Power BiCMOS Current-Mode PWM data sheet, (SLUS270)
3. PowerPAD™ Made Easy, Application Brief, (SLMA004)
4. Predictive Gate Drive™ Boosts Synchronous Rectifier Efficiency, by Steve Mappus, (SLUA281)
5. UCC27221/2 Predictive Gate Drive™ FAQ's, by Steve Mappus, (SLUA280)
6. 12-V to 1.8-V, 20A High-Efficiency Synchronous Buck Converter Using UCC27222 with Predictive Gate Drive™ Technology, by Steve Mappus, UCC27222EVM user's guide, (SLUU140)
7. Low Voltage Feedback in PWM Applications, by Steve Mappus, application note, (SLUA286)

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